[See Signature Page for Information on Counsel for Plaintiffs]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **NOTICE OF MOTION AND MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF FIRST CLAIM CONSTRUCTION ORDER; MEMORANDUM OF POINTS AND AUTHORITIES** **[RELATED CASES]** Date: November 30, 2012 Time: 10:00 a.m. Place: Courtroom 5, 4th Floor Judge: Paul Singh Grewal
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-05398 PSG

TABLE OF CONTENTS

TABLE OF AUTHORITIES

PAGE(S)

CASES

PLEASE TAKE NOTICE that declaratory relief plaintiffs Acer, HTC and Barco entities as shown on the caption page (collectively "Plaintiffs"), pursuant to Civil Local Rule 7-9, hereby respectfully file a Motion for Reconsideration of Certain Aspects of First Claim Construction Order. Plaintiffs' Motion is based on this Notice of Motion and Motion and the record of the Court, and upon such other matters as may be presented to the Court. The Motion is scheduled to be heard on November 30, 2012 at 10:00 a.m.

The undersigned bring this Motion to seek reconsideration of certain aspects of the First Claim Construction Order issued on June 12, 2012. (Dkt. No. 336, Case No. 5:08-cv-00877 PSG ("*Acer* Action") ("Order").) In particular, Plaintiffs request that the Court (1) construe the claim term "supply the multiple sequential instructions to said central processing unit during a single memory cycle" that Judge Ware declined to construe and (2) construe the term "clocking said central processing unit" in light of prosecution history disclaimers that Judge Ware did not consider.

I. JUDGE WARE MISUNDERSTOOD THE REAL ISSUE IN DISPUTE WHEN DECLINING TO CONSTRUE THE "SUPPLY THE MULTIPLE SEQUENTIAL INSTRUCTIONS . . . " PHRASE FROM THE '749 PATENT

Judge Ware declined to construe the term "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" due to a misunderstanding of the disputed issue. (Order at 8–9.) Judge Ware stated, or rather misstated, that "the issue tendered to the Court is whether the phrase should be defined as **requiring a 'prefetch buffer.'**" (*See id.* (emphasis added).) Judge Ware then noted that, "[u]pon review, the Court does not find that the cited statements constitute a basis for construing the language of Claim 1 to include the presence or configuration of a prefetch buffer. Having disposed of the only issue tendered with respect to this phrase, the Court declines to further construe it." (*Id.*)

But no party asserted that this disputed phrase ***required*** the inclusion of a prefetch buffer. In fact, Plaintiffs' position was just the opposite—that this term must be defined as *excluding* a "prefetch buffer" that supplies instructions to the CPU *one at a time*, which was unambiguously disclaimed during prosecution. (Pls.' Consol. Resp. Claim Constr. Brief at 27–28, Dkt. No. 319, *Acer* Action.)

The parties have proposed the following proposed constructions for the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle":

Plaintiffs' Construction	TPL's Construction
provide the multiple sequential instructions in parallel **(as opposed to one-by-one)** to said central processing unit integrated circuit during a single memory cycle **without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies one instruction at a time**	provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

The actual disputed issue is whether this term should exclude supplying instructions *one at a time* to the CPU, not whether a prefetch buffer is required. As explained below, during the reexamination of the '749 patent, TPL told the PTO on at least four occasions that this claim term is **not** satisfied by a system that supplies instructions one-at-a-time to the CPU (for example, through the use of a prefetch buffer). (*Id.*) Whether or not a "prefetch buffer" is present is merely collateral to the real issue of whether TPL must be held to the clear disclaimers during reexamination of supplying instructions *one at a time* to the CPU.

A. Background of the '749 Patent

The disputed phrase "supply multiple sequential instructions to central processing unit integrated circuit during a single memory cycle" is recited in claim 1 of U.S. Patent No. 5,440,749 ("'749 patent" (Declaration of Kyle Chen ("Chen Decl."), Ex. 1) , which purports to describe a high-performance, low-cost microprocessor system. ('749, 1:7–13.) The central processing unit ("CPU") described in the '749 patent operates by fetching "instructions" from memory and then executing them. These fetched instructions specify the operations the CPU will perform. The '749 patent explains, however, that "[t]he slowest procedure the microprocessor 50 performs is to access memory." ('749, 22:14–17.) "Memory is accessed when data is read or written. Memory is also read when instructions are fetched." *Id.* "The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data." ('749, 5:54–56.)

The '749 patent purports to address this "bottleneck" problem through a microprocessor system that has the ability to fetch *multiple* instructions from memory and supply them to the

CPU during "a single memory cycle," *i.e.*, the period of time required to perform one memory access. Because the CPU can execute instructions much faster than it can fetch them from the memory, allowing multiple instructions to be fetched and supplied to the CPU during a single memory cycle can improve performance by permitting the fetching and execution of instructions to take place in parallel. (*See* '749, 22:17–40.) The specification of the '749 patent repeatedly touts the perceived advantages of this feature. ('749, 18:10–12 ("The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access."); *see also, e.g.*, '749, 7:12–18; 5:54–58.)

The two asserted independent claims of the '749 patent (*i.e.*, claims 1 and 9) include a substantially identical limitation directed to this feature. In particular, each independent claim requires that the microprocessor system be configured to fetch multiple sequential instructions in parallel and *supply them to the CPU during a single memory cycle*. Claim 1 of the '749 patent, as amended following the reexamination of the '749 patent, is reproduced below (the disputed claim language shown in bold underlining, reexamination amendments shown in italics):

> 1. A microprocessor system, comprising a central processing unit integrated circuit, a memory extend of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and **supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle**, said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel, said central processing unit *integrated circuit* including an arithmetic logic unit and a first push down stack connected to said arithmetic, logic unit, [sic] said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack said arithmetic logic unit having an output connected to said means for storing a top item, *wherein the microprocessor system comprises an instruction register configured to store the multiple sequential*

> *instructions and from which instructions are accessed and decoded; and wherein the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.*

('749, Ex Parte Reexamination Certificate, Claim 1 (bold and underlining added; italics in original reexamination certificate) (Chen Decl., Ex. 1).) Claim 9 contains substantially the same requirement. (*See* '749, claim 9 ("said means for fetching instructions being configured to . . . supply the multiple instructions to said central processing unit during a single memory cycle").) Although claim 9 was cancelled during the '749 reexamination, all of its limitations—including the one at issue here—were incorporated into substituting and dependent claims.

B. TPL Affirmatively and Repeatedly Disclaimed Systems that Supply Instructions to the CPU One at a Time During the Reexamination.

On November 19, 2009, the PTO issued an Office Action in the reexamination rejecting various claims of the '749 patent (including claim 1) based on U.S. Patent No. 4,680,698 to Jonathan Edwards ("Edwards") and an article entitled *The Motorola MC68020* by Doug MacGregor *et al.* ("MacGregor"). As explained below, in attempts to distinguish Edwards and MacGregor, TPL unequivocally disclaimed systems that supply instructions to the CPU one-at-a-time by arguing that those systems do not "supply the multiple sequential instructions to the CPU during a single memory cycle," as required by the claims of the '749 patent. TPL is bound by those disavowals. Therefore, systems that operate in that manner cannot infringe the claims.

Specifically, on January 19, 2010, in its attempt to distinguish its claims over the prior art, TPL told the PTO why Edwards did not disclose this element:

> Edwards describes the way the Transputer decodes and executes instructions. As described in Edwards, see, e.g., Fig. 8, below, <u>instructions are supplied to a one-instruction-wide instruction buffer, one at a time</u>, and are there decoded. <u>Fetching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation – the supplying of "multiple sequential instructions to a CPU during a single memory cycle</u>."

(Amendment, 1/19/10, p. 26 of 58, Chen Decl., Ex. 2 (emphasis added).) TPL made a similar disclaimer in distinguishing the claimed invention from MacGregor:

> However, [MacGregor] does not disclose fetching "multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle." MacGregor might imply that it fetches two instructions from memory at a time, but the instructions are supplied to the CPU one at a time. Such non-parallel supplying of instructions to the CPU is not supplying them to the CPU during a single memory cycle as required by the claim.

(*Id.*, p. 45 of 58.)

On September 29, 2010, the PTO issued a final Office Action maintaining the rejection of claims 1 and 9. Shortly thereafter, TPL conducted an interview with the Examiner. Following that interview, TPL filed a written summary of its arguments and reaffirmed that systems supplying instructions to the CPU one at a time were *not* covered by the claims of the '749 patent:

> Next the MacGregor reference was discussed [during the interview]. Mr. Henneman[, TPL's counsel,] explained that although two instructions might be fetched at the same time, only one instruction is supplied to the CPU at a time. The second instruction is stored in a temporary register. Because MacGregor only discloses providing instructions to the CPU one-at-a-time, Examiner Pokrzwya indicated that he would reconsider this rejection.

(Amendment, 11/29/10, pp. 19–20 of 35, Chen Decl., Ex. 3 (emphasis added).) Additionally:

> As discussed in the interview and elaborated on above with respect to the May/Edwards rejections, the "during a single memory cycle" limitation is not satisfied by supplying only one instruction to a CPU at a time. Rather, the "multiple sequential instructions" must be supplied "during a single memory cycle."

(*Id.* at p. 31 of 35 (emphasis added).) The PTO subsequently issued a Notice of Intent to Issue a Reexamination Certificate as to the '749 patent.

Each of TPL's disclaimers must be taken into account in a proper claim construction. "The purpose of consulting the prosecution history in construing a claim is 'to exclude any interpretation that was disclaimed during prosecution.'" *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (citation omitted). "Accordingly, 'where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of

the surrender.'" *Id*. (citation omitted); *see also, e.g.*, *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to narrow claim interpretations because 'the public has a right to rely on such definitive statements made during prosecution.'") (citation omitted). The principle that a patent owner is bound to its representations to the PTO serves a critical purpose. "Such a use of the prosecution history ensures that claims are not construed one way in order to obtain their allowance and in a different way against accused infringers." *Chimie*, 402 F.3d at 1384.

It is hard to imagine a clearer case of prosecution disclaimer than the one presented above, in which TPL repeatedly told the PTO precisely what was not covered by its claims. TPL not only pointed to specific features of the prior art but directly linked them to the disputed phrase "supply the multiple sequential instructions to said central processing unit during a single memory cycle." TPL's arguments did not turn on the presence or absence of any particular device or structure (such as a prefetch buffer), as TPL misleadingly argued to Judge Ware, but on the fact that the claimed invention does not cover supplying instructions *one at a time* to the CPU. Plaintiffs' proposed construction does incorporate language excluding a "prefetch buffer" and a "one-instruction-wide instruction buffer," but only because these structures were specifically disclaimed by TPL in its statements. The overarching and broader theme of TPL's arguments to the PTO was that this phrase excludes supplying instructions *one-by-one* to the CPU—regardless of the structure or component employed. Plaintiffs therefore respectfully request that the Court construe this phrase as providing the multiple sequential instructions "in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle without using a prefetch buffer or a one-instruction-wide buffer that supplies one instruction at a time," as Plaintiffs have proposed.

C. TPL Cannot Be Allowed to Recapture Disclaimed Subject Matter.

As explained above, TPL plainly told the PTO that the requirement of supplying multiple sequential instructions to the CPU during a single memory cycle "is not satisfied by supplying only ***one instruction*** to a CPU ***at a time***." (Amendment, 11/29/10, p. 31 of 35, Chen Decl., Ex. 3 (emphasis added).) TPL's infringement contentions as to this element, however, affirmatively

allege that the accused products supply instructions *one-at-a-time* to the CPU in precisely the same manner as the prior art TPL disclaimed.

All of the products accused by TPL in this action use chips that incorporate microprocessor cores provided by a third party, ARM Ltd. ("ARM cores"). ARM cores, the alleged "central processing unit" according to TPL's infringement contentions, execute either 32-bit ARM instructions or a more compact instruction set referred to as "Thumb" instructions. Each Thumb instruction is 16-bits in length, such that two 16-bit Thumb instructions fit within a single 32-bit unit (known as a "word"). TPL claims that the accused products satisfy the element of supplying "multiple sequential instructions" to the CPU "during a single memory cycle" because they can fetch, during a single memory cycle, a 32-bit word containing two 16-bit Thumb instructions. But critically, TPL's infringement contentions go on to concede that these 16-bit instructions are supplied to the CPU one-at-a-time. For example, in the cell of its infringement charts corresponding to the claim limitation "supply the multiple sequential instructions to said central processing unit during a single memory cycle," TPL alleges:

> The ROM [*i.e.*, read-only memory] stores a mixture of routines of 32-bit ARM code with one instruction per 32-bit word and routines of Thumb code with two instructions per word. Each external fetch draws either one 32-bit ARM instruction or two 16-bit Thumb instructions. ARM instructions flow into the core pipeline in the usual way. However, in Thumb state, ***one Thumb instruction*** goes into the pipeline while the other is stored on a 16-bit latch, which is effectively a one-instruction prefetch buffer. At ***the next fetch***, this stored instruction is immediately available to the core.

(Chen Decl., Ex. 4, pp. 6 and 14 of 24 (emphasis added) (quoting ARM Ltd., *An Introduction to Thumb*).) TPL's infringement contentions rely on the above-quoted factual allegation to explain how the handling of two Thumb instructions in a "word" allegedly meets this claim element. That mechanism, however, supplies only ***one*** of the two Thumb instructions to the CPU's "pipeline" at first, while the other is temporarily stored in the "prefetch buffer." Such other temporarily stored Thumb instruction is not supplied to the CPU (*i.e.*, the "core") until the "next fetch." That is, the two Thumb instructions are supplied to the CPU ***one at a time***, just like the prior art distinguished by TPL during the '749 reexamination.

The construction of this phrase is potentially dispositive of the '749 patent. By declining to construe this phrase and misunderstanding the issue, Judge Ware created the possibility that TPL could continue to accuse products of infringement, notwithstanding that they exhibit the precise characteristic that was essential for distinguishing the claims over the prior art. As the Federal Circuit has noted, "[t]he public has a right to rely on the assertions made by a patent applicant to secure allowance of its claims. Post-hoc, litigation-inspired argument cannot be used to reclaim subject matter that the public record in the PTO clearly shows has been abandoned." *Desper Prods., Inc. v. QSound Labs, Inc.*, 157 F.3d 1325, 1340 (Fed. Cir. 1998). Thus, TPL should not be permitted to recapture, through claim construction, a claim scope covering the very embodiments it surrendered during reexamination.

II. JUDGE WARE ERRED BY NOT CONSIDERING THE PATENT OWNER'S PROSECUTION HISTORY DISCLAIMERS WHEN CONSTRUING THE "CLOCKING SAID CPU" PHRASE FROM THE '336 PATENT.

In construing the term "clocking said CPU," Judge Ware's Order did not consider the patent owner's disclaimers made during prosecution of U.S. Patent No. 5,809,336 ("'336 patent") (Chen Decl., Ex. 5) in light of the specification. As a result, the term was erroneously construed as "providing a timing signal to said central processing unit." (Order at 18.) Judge Ware's Order devoted only a few sentences to this phrase, concluding that "[a] description of **an embodiment in the specification** may not be imposed as a limitation" absent clear intent. (Order at 17–18 (emphasis added) (citation omitted).) Plaintiffs respectfully submit that Judge Ware's construction of this phrase warrants reconsideration for at least the following three reasons. First, Judge Ware appears to have focused exclusively on the specification, but the patent owner made statements in *both* the specification *and the prosecution history* showing that the CPU in the '336 patent must be clocked such that it will always execute at the maximum frequency possible. Second, Judge Ware also appears to have been under the misimpression that the clocking circuit in the specification was merely "an embodiment" among others. But as shown below, it is the ***sole*** embodiment in the specification and was repeatedly characterized as "the present invention" during the '336 prosecution. Third, the combination of the specification and the prosecution history exhibits a clear intent to limit the alleged invention to a system that ***always*** clocks the

CPU at its maximum speed, and Judge Ware's erroneous construction will result in recapture of subject matter surrendered during prosecution to gain allowance.

Because the disputed phrase "clocking said CPU" appears in every independent claim of the '336 patent, this phrase is potentially dispositive of this patent and thus should receive full consideration in light of the entire record, including both the specification and the prosecution history.

A. Background of the '336 Patent

The '336 patent discloses a microprocessor system with a variable speed clocking system that purports to achieve maximum performance under various and changing environmental conditions. The specification criticizes prior art microprocessor designs for restricting the CPU to a fixed or "rated" clock speed in order to ensure proper operation under the worst-case conditions:

> The designer of a high speed microprocessor must produce a product which operate [sic] over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse [sic] case of the three parameters, the circuit will function at the rated clock speed. The result are [sic] designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse [sic] case conditions.

('336, 16:44–53.)

The '336 patent explains that the speed of traditional CPUs is locked to the fastest speed for the CPU to operate properly under worst-case environmental parameters (such as temperature). (*Id.*) Thus, the CPU designs of the prior art would only sometimes operate at their fastest speed (*i.e.*, under worst-case conditions). Because environmental parameters will frequently ***not*** reach worst-case conditions, much of the CPU's potential computing power is lost.

For example, the specification describes a "ring oscillator" system clock that can time the CPU at a frequency in the neighborhood of 100 MHz under room temperature, but at only 50 MHz under a higher temperature of 70º C. ('336, 16:62–63.) Assuming a worst-case temperature of 70º C, the traditional approach disparaged in the '336 patent would lock the CPU clock to a frequency of 50 MHz at all times to ensure proper operation under any temperature up to 70º C—although the CPU could be clocked at *twice* that speed under room temperature. ('336, 16:60–62.)

The '336 patent purports to address this problem by placing the "ring oscillator" system clock on the same chip as the CPU. ('336, 16:56–58 ("Clock circuit **430** is the familiar 'ring oscillator' used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor **50**.").) According to the '336 patent, because this "ring oscillator" system clock is placed on the same chip as the CPU, the performance deficiencies of the traditional "rated clock speed" CPUs can now be overcome by this variable speed clock that always achieves maximum speed under any environment, not just in worst-case scenarios:

> The ring oscillator **430** is useful as a system clock . . . because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring oscillator **430**, CPU **70** will always execute at the maximum frequency possible, but never too fast.

('336, 16:63–17:2; *see also id.*, 17:19–21 ("The CPU **70** executes at the fastest speed possible using the adaptive ring counter[1] clock **430**.").)

The "ring oscillator" described above is the sole embodiment in the specification for clocking the CPU. ('336, 16:44–17:37). TPL nonetheless misleadingly told Judge Ware that "[t]he specification of the patents-in-suit discloses multiple embodiments of the various inventions; so many that the PTO required the applicants to divide the original application into 10 separate applications." (Defs.' Reply Cl. Constr. Brief at 7, Dkt. No. 322, *Acer* Action (citation omitted).) Those other "embodiments," however, are not directed to the on-chip CPU clock and are therefore irrelevant to the construction of this phrase. The "ring oscillator" described above is incontrovertibly the only embodiment in the specification and the sole support for the "clocking said CPU" phrase.

B. Applicants Repeatedly Cited the Feature of Always Clocking the CPU at Its Maximum Speed as a Feature of the "Present Invention."

The applicants reiterated, through the original prosecution history of the '336 patent, that "clocking the CPU" meant timing its operation such that it will always execute at the maximum

[1] The parties have agreed that "ring counter" is the same as "ring oscillator." (*See* Ex. A to Pls.' Consolidated Responsive Claim Construction Brief at 2, no.10, Dkt. No. 334-01, Case No. 5:08-cv-0882 PSG.)

possible frequency. For example, the applicants relied on this feature to distinguish U.S. Patent No. 4,670,837 to Sheets (Chen Decl., Ex. 6) ("Sheets"):

> Specifically, Claims 19 and 65 now explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit. Moreover, these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock:
>
> > . . . **The CPU 70 executes at the fastest speed possible** using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. (page 32, lines 10-13)
>
> **Neither of these aspects of the 'present invention' are suggested by Sheets.**

(Amendment, 4/15/96, pp. 8–9, Chen Decl., Ex. 7 (emphasis and quotation marks added).)

Application claims 19 and 65 referenced above respectively issued as claims 1 and 3 of the '336 patent that include the term "clocking said CPU." (*See* Chen Decl., Ex. 9.) The applicants again identified and relied on this feature to distinguish prior art in a later written submission:

> In the interview, the fact that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit was discussed… This fact is utilized in **the present invention** to provide a variable speed clock for the microprocessor, with the clock speed varying in the same way as variation in the operating characteristics of the electronic devices making up the microprocessor. **This allows the microprocessor to operate at its fastest safe operating speed**, given its manufacturing process or changes in its operating temperature or voltage. **In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operation conditions** and an external clock is used to drive them no faster than the rated speed. **Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.**

(Amendment, 1/13/97, pp. 3-4, Chen Decl., Ex. 8 (emphasis added).)

Because the "rated speed" in prior art microprocessor systems is set "based on possible worst case operation conditions," that rated speed represents the fastest possible speed ***only*** when the environmental conditions are at their worst. In other words, prior art systems operate at their

maximum performance only sometimes (*i.e.*, when under worst-case conditions), but not always, which is the issue the '336 patent attempts to address. (*See id.*)

Both in the specification and echoed in the prosecution history cited above, the applicants repeatedly criticized prior art CPU designs that locked CPU frequency to a rated clock speed because they did not always clock the CPU at its maximum frequency possible. The applicants thereby clearly and unmistakably disclaimed coverage of systems in which the CPU does not always execute at the maximum frequency possible. *See, e.g., Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1333 (Fed. Cir. 2009) ("Where the general summary or description of the invention describes a feature of the invention . . . and criticizes other products . . . that lack that same feature, this operates as a clear disavowal of these other products . . . .") (citation omitted); *see also Peavey Elec. Corp. v. Behringer Int'l GMBH*, No. 09-918 (JLL), 2010 WL 4669907, at *10 (D.N.J. Nov. 9, 2010) ("As discussed above, during the prosecution of the '428 Patent, in order to overcome an obviousness rejection, Peavey clearly and deliberately: (1) criticized prior art circuits which turned on multiple lights at any given point in time . . . ."); *see also Paragon Solutions, LLC v. Timex Corp.*, 566 F.3d 1075, 1092 (Fed. Cir. 2009) ("The applicants' remarks distinguishing Root [during prosecution] therefore echo the criticism of the prior art in the specification.").

C. Features of the "Present Invention" Used to Overcome Prior Art Must Limit the Claim Scope.

"Where an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of otherwise broad claim language." *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372–73 (Fed. Cir. 2005). Here, the prior art systems in which the CPU did not always execute at its maximum frequency were repeatedly distinguished in both the specification and the prosecution history. The applicants were adamant that their invention was different from the prior art because the CPU always executed at the maximum frequency possible. The prosecution history also repeatedly describes this feature of clocking the CPU at its fastest speed as part of "the present invention," as shown above. While the disclosure of just one single embodiment in the

specification, as here, does not necessarily limit the scope of the claims, that single embodiment here was repeatedly described in the applicants' arguments during prosecution as "the present invention." *Cf. Honeywell Int'l, Inc. v. ITT Indus.*, 452 F.3d 1312, 1317–19 (Fed. Cir. 2006) (limiting the broader claim term "fuel injection system component" to "fuel filter," where a fuel filter was **the only component** disclosed in the written description and was described as "**the present invention**") (emphasis added); *see also Edwards Lifesciences LLC*, 582 F.3d at 1331 (embodiment described as "the invention" or "present invention" in specification may limit claims to what is described as such). Thus, the claims should require that the CPU executes at the maximum frequency possible, and therefore, Plaintiffs' proposed construction should be adopted.

D. TPL Cannot Be Allowed to Recapture Disclaimed Subject Matter.

As explained above, based on the specification and the prosecution history, the term "clocking said CPU" should be construed to exclude the prior art systems that operate at the fastest possible speed only under worst-case conditions. To avoid recapturing surrendered subject matter, this term must be given a construction requiring that the CPU "always" clock the CPU at the fastest possible speed. *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1374-75 (Fed. Cir. 2008) ("The doctrine of prosecution disclaimer 'protects the public's reliance on definitive statements made during prosecution' by 'precluding patentees from recapturing through claim interpretation specific meanings [clearly and unmistakably] disclaimed during prosecution.") (brackets in original) (citation omitted); *see also Desper Prods., Inc.*, 157 F.3d at 1340 ("The public has a right to rely on the assertions made by a patent applicant to secure allowance of its claims. Post-hoc, litigation-inspired argument cannot be used to reclaim subject matter that the public record in the PTO clearly shows has been abandoned."). Plaintiffs therefore respectfully request that Judge Ware's construction be revisited, and the "clocking said CPU" phrase be construed to mean: "timing the operation of the CPU such that it will always execute at the maximum speed possible, but never too fast," as Plaintiffs have proposed.

III. CONCLUSION

For the foregoing reasons, Plaintiffs respectfully request that the Court grant its Motion for Reconsideration of Certain Aspects of First Claim Construction Order in its entirety.

Dated: October 19, 2012

K&L GATES LLP

By: */s/ Timothy Walker*

Timothy P. Walker, Esq.
Timothy.walker@klgates.com
Howard Chen, Esq.
Howard.chen@klgates.com
Harold H. Davis, Jr., Esq.
Harold.davis@klgates.com
Jas Dhillon, Esq.
Jas.dhillon@klgate.com
Jeffrey M. Ratinoff
Jeffrey.ratinoff@klgates.com
K&L Gates LLP
Four Embarcadero Center, Suite 1200
San Francisco, CA 94111
Phone: (415) 882-8200
Fax: (415) 882-8220

Attorneys for Acer, Inc., Acer America Corp. and Gateway, Inc.

Dated: October 19, 2012

COOLEY LLP

By: */s/ Kyle D. Chen*

Kyle D. Chen, Esq.
kyle.chen@cooley.com
Heidi L. Keefe, Esq.
hkeefe@cooley.com
Mark R. Weinstein, Esq.
mweinstein@cooley.com
Cooley LLP
3000 El Camino Real
Five Palo Alto Square, 4th Floor
Palo Alto, California 94306
Phone: (650) 843-5000
Fax: (650) 857-0663

Attorneys for HTC Corporation and HTC America, Inc.

Dated: October 19, 2012

BAKER & MCKENZIE

By: */s/ Edward Runyan*

Edward Runyan, Esq.
Edward.Runyan@bakernet.com
Baker & McKenzie
130 East Randolph Drive
Chicago, IL 60601
Phone: (312) 861-8811
Fax: (312) 698-2341

Attorneys for Barco, N.V.

ATTESTATION PER GENERAL ORDER 45

I, Kyle Chen, am the ECF User whose ID and password are being used to file Plaintiffs' Motion for Leave to file Motion for Reconsideration of Certain Aspects of First Claim Construction Order. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

Dated: October 19, 2012

By: */s/ Kyle Chen*
Kyle Chen